ECE Department
TEZPUR University

Chips to Startup Programme

Two-Day Training on Full custom & Semi-Custom IC Design Flow Using Cadence EDA Tools

Organized by C2S Program Team at Tezpur University

9th -10th September 2025

REGISTRATION & ELIGIBILITY

Total seats available: 15
Limited Seats (First-come, First-Serve)

Free Registration

B.Tech 5th & 7th Semester

M.Tech (ELDT,SCT, Bio)

TRAINER:

Entuple Technologies Pvt Ltd. Team

VENUE:

**VLSI Lab, ECE Dept.
Tezpur University**

CONTACT & REGISTRATION:

Coordinator: Dr. Kasturi Gogoi

https://forms.gle/ottpowHBwWaXMvW99

Session 1
10:00 am - 01:00 pm

Session 2
02:00 pm - 04:00 pm

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Day 1: Full Custom IC Design Flow

Session 1 (10 am - 1 pm)

- Introduction to Full Custom IC Design Flow
- Cadence Solutions for Custom IC
- MOSFFT Characterization
- Schematic Capture
- Usmersin Creation
- Testbonch Creation

Session 2 (2 pm - 4 pm)

- Layout Design (Virtuoso Layout Editor)
- Physical Verification (DRC & LVS)
- Parsaitic Extraction (Quantus)
- Post Layout Simulation
- GDSII Generation

Note: By considering, CMOS INVERTER **as an example will demonstrate the entire Full Custom IC Design Flow.**

Day 2: Semi-Custom IC Design Flow

Session 3 (10 am - 1 pm)

- Introduction to Semi-Custom IC Design Flow
- Cadence Solutions for Semi-Custom IC Design
- Functional Verification using Incisive
- RTL Synthesis using Genus Synthesis Solution

Key Takeaways

- Hands-on training with Cadence EDA Tools
- Full Custom & Semi-Custom IC Design Flow
- Industry-standard Simulation & Verification
- Mentorship from Entuple Technologies Pvt Ltd. Expert Team